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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,701	12/10/2001	Andrew Douglas Davies	ROC920010056US1	4420

7590 06/17/2004

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,701	DAVIES ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on December 10, 2001 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims rejected under 35 U.S.C. 102(b) as being anticipated by "*Scan Synthesis for One-Hot Signals*" by Mitra et al. International Test Conference Proceedings, 1-6 Nov. 1997, page 714 – 722, Inspec Accession Number: 5863303.

As per claims 1 and 7-9, Mitra et al. teach that in a scan-path based design, the circuit has two operating modes: normal functional mode, and scan mode, during which the circuit bistables are interconnected into a shift register. In the scan mode, it is possible to shift an arbitrary test pattern into the bistables. By returning the circuit to normal mode for one clock period, the outputs of the combinational circuitry are stored in the bistables. It the circuit is then placed into scan mode it is possible to shift out the

contents of the bistables and compare these contents with the correct response. Thus, a sequential circuit is transformed into a combinational one during testing thereby making test generation simpler. Many circuits contain logic that is controlled by one-out-of-n (one-hot) input signals. A typical example is an n-to-l multiplexer implemented with n transmission states, each enabled by a different control signal. Tri-state buses and logic implemented with pass transistors are typically used in complex microprocessors to achieve high performance in a small area. Unfortunately, the presence of tristate buses and pass transistor logic poses a problem in a scan or BIST design. At some point during the testing process, the bistables may contain a state that does not occur during functional operation, and this can result in non-one-hot values on the one-hot signals. Bistables may contain invalid state: while patterns are scanned in and out or when pseudo-random patterns are applied to the circuit during BIST operation. This can result in abnormal and unpredictable, circuit behavior. In designs containing tristate buses, the presence of non-one-hot values in the tristate control inputs may cause circuit damage. The goal is to generate one hot signals that are safe for scan and BIST operations. (page 714 section 1 pp 1-4, page 715 section 2 pp 2 (last 12 lines), Fig. 4)

As per claims 3 and 5, Mitra et al. teach using a testable design with test signals controlled by 1 out of n signals (page 721 section 7 pp1)

As per claim 6, Mitra et al. teach gate the output of the one-hot bistables during scam with a scan signal, resulting in a particular one-hot value enforced on the bistable outputs irrespective of their contents. Only one of the bistable outputs should be or-ed

with the scan signal while the other latch outputs should be and-ed with the (scan)' signal. (page 714 section 2 pp1)

As per claims 10, and 11, Mitra et al. teach that the encoding logic has *n* inputs corresponding to the *n* one-hot signals and produces *n* one-hot output signals. If the input to the encoder is one-hot, then the encoder output should be the same as the input. If the encoder input is not once-hot, the encoder can map it to any one-hot value. A typical example of such encoding logic is a *priority encoder* which produces a 'l' on output i and `0' on the remaining; outputs if all inputs 1..., i-l are '0', input i is '1'. Thus, the priority encoder ensures that, as long as it is fault-free, its outputs are one-hot. (Fig. 1. page 715, column 1 pp 2,)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over "*Scan Synthesis for One-Hot Signals*" by Mitra et al. International Test Conference Proceedings, 1-6 Nov. 1997, page 714 – 722, Inspec Accession Number: 5863303, in view of Beausang et al. U. S. Patent No. 6,012,155.

As per claims 2 and 4, Mitra et al. teach that in a scan-path based design, the circuit has two operating modes: normal functional mode, and scan mode, during which the circuit bistables are interconnected into a shift register. In the scan mode, it is possible to shift an arbitrary test pattern into the bistables. By returning the circuit to normal mode for one clock period, the outputs of the combinational circuitry are stored in the bistables. It the circuit is then placed into scan mode it is possible to shift out the contents of the bistables and compare these contents with the correct response. Thus,

a sequential circuit is transformed into a combinational one during testing thereby making test generation simpler. Many circuits contain logic that is controlled by one-out-of-n (one-hot) input signals. A typical example is an n-to-l multiplexer implemented with n transmission states, each enabled by a different control signal. Tri-state buses and logic implemented with pass transistors are typically used in complex microprocessors to achieve high performance in a small area. Unfortunately, the presence of tristate buses and pass transistor logic poses a problem in a scan or BIST design. At some point during the testing process, the bistables may contain a state that does not occur during functional operation, and this can result in non-one-hot values on the one-hot signals. Bistables may contain invalid state: while patterns are scanned in and out or when pseudo-random patterns are applied to the circuit during BIST operation. This can result in abnormal and unpredictable, circuit behavior. In designs containing tristate buses, the presence of non-one-hot values in the tristate control inputs may cause circuit damage. The goal is to generate one hot signals that are safe for scan and BIST operations. (page 714 section 1 pp 1-4, page 715 section 2 pp 2 (last 12 lines), Fig. 4). Not explicitly disclosed is that either all zeros or all ones can be used in the scan.

However, in an analogous art, Beausang et al. teach "there is no inversion of data between the TDI and TDO of any TDR; the behavior of the IR 655 during each TAP controller state; the latching of the instruction on the falling edge of TCK; the all zeros instruction corresponds to EXTEST; the all ones instruction corresponds to BYPASS; the length of the bypass register 416 and its capture value" (column 12 line

60 through column 13 line 7). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the all ones or all zeros of Beausang et al. with the one hot methods of Mitra et al. this would have been obvious as suggested by Beausang et al. (column 3 lines 21-25) in order to reduce processing time of the instructions.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 4,057,693 Angner et al.

This patent teaches signals from the input buffers and timer control the states of the flip-flops. The circuit is designed so that only one flip-flop is set at a time (one-hot coding). Each flip-flop relates directly to a line circuit state: IDLE (I), RING (R), BUSY (B1 and B2) and HOLD (H). The state outputs are decoded by output translation logic and are also fed back to the two timers. The main timer on the chip contains a 4-bit binary ripple counter and associated enable and clock control circuitry. The state outputs from the 5-State Asynchronous Machine, signals from the Input Buffers, and the output from Timer 32 control when and at what rate Timer 31 counts. Four timer outputs control the state transitions within the 5-State Asynchronous Machine and the HOUT buffer in the Output Logic and Buffers circuitry.

U. S. Patent No. 6,081,913 and 5,898,702 Narayanan et al.

These patents teach a method for controlling a gating circuit of an electronic system incorporating a scan architecture complying with IEEE Standard 1149.1 (or locally ensuring mutual exclusivity to selected signals during scan testing such that the gating circuit applies mutually exclusive signals to, for example, a decoded multiplexer. The gating circuit receives input signals from flip-flops that are part of a scan chain, is selectively controllable by a control signal to transmit predetermined mutually exclusive signals to the select inputs of the multiplexer during a scan mode. Alternatively, the gating circuit is controllable by the control signal to pass the input signals to the multiplexer in a normal operation or test mode. A mutual exclusivity circuit is provided to generate the control signal. During the scan mode, the control signal is generated at a first logic level such that the gating circuit transmits the predetermined mutually exclusive signals to the multiplexer while test values are being scanned into the flip-flops. Upon transition from the scan mode to the normal operation mode, the control signal is changed to a second logic level for a predetermined time period, and then changed back to the first logic level. When the control signal is at the second logic level, the gating circuit passes the input signals to the multiplexer, and the electronic system operates to propagate response signals that are applied to, for example, the scan chain flip-flops. In some instances, these response signals received by the flip-flops are not mutually exclusive, and the multiplexer may be damaged. The predetermined time period is set to apply the predetermined mutually exclusive signals before this possible damage occurs.

U. S. Patent No. 6,735,731 Ewen et al.

This patent teaches an (n+1) bit one-hot ripple counter, wherein (n+1) bit corresponds to the total number of channels (e.g., channel 0 to channel n) being tested (e.g., an eleven-bit ripple counter for a twelve channel parallel optical transceiver). A counter or poll clock signal may be utilized as the input signal to the counter to set the counter speed. In one embodiment, the poll clock signal is sufficiently slow (e.g., less than about 120 Hz) to allow human observation of the error status and selected channel. The output of the counter is connected to the select of the channel multiplexer, which then selectively outputs the error status of the selected channel.

U. S. Patent No. 6,490702 Song et al.

This patent teaches a scan chain latch circuit which includes a first shift register latch and a second shift register latch. The scan chain latch circuit also includes a multiplexor connected between the first and second shift register latches, the multiplexor has a select line for controlling the function of the multiplexor. The multiplexor is configured for implementing an inverting mode such that a logic value may be passed via the multiplexor from the first shift register latch to the second shift register latch in one of a non-inverted state and an inverted state based upon the state of the select line.

"*Delay-Fault Test Generation and Synthesis for Testability Under A Standard Scan Design Methodology*" Cheng et al. IEEE Transactions on Computer-Aided Design of Inspec Accession Number: 4567801

This paper teaches the problems of test generation and synthesis aimed at producing VLSI sequential circuits that are delay-fault testable under a standard scan design methodology. Theoretical results regarding the standard scan-delay testability of finite state machines (FSMs) described at the state transition graph (STG) level are given. It is shown that a one-hot coded and optimized FSM whose STG satisfies a certain property is guaranteed to be fully gate-delay-fault testable under standard scan. This result is extended to arbitrary-length encodings, and a heuristic state assignment algorithm that results in highly gate-delay-fault testable sequential FSMs is developed. A version of the scan shifting technique is also used in the test pattern generator. Test generation, flip-flop ordering, flip-flop selection and test set compaction results on large benchmark circuits are presented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

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